Multi-channel readout electronics for silicon PIN diodes

based on SKIROC2 ASIC

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**Abstract:**

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# Introduction

Silicon PIN diode plays an important role in photoelectric conversion. Thanks to the fine resolution of energy and position, it has been widely used in high-energy physics experiments such as the CALorimetric Electron Telescope (CALET) and the International Linear Collider (ILC)1 2. The Circular Electron Positron Collider (CEPC) also takes silicon-tungsten-based Electromagnetic CALorimeter (Si-W ECAL) as a promising solution for the high-granular calorimetry3. The use of silicon PIN diode tends to be highly integrated4, leading to a requirement for multi-channel readout electronics.

The Silicon Kalorimeter Integrated ReadOut Chip 2 (SKIROC2) is an ASIC developed in the CALICE collaboration for the readout of silicon PIN diodes5. The SKIROC2 integrates 64 channels on one chip and has the feature of low noise and large dynamic range. A multi-channel readout electronics, based on SKIROC2 ASIC, was designed and implemented. A kind of silicon PIN diode named S5980 from HAMAMATSU was coupled with the electronics to test its performance. Details of the readout electronics and test results are presented below.

# Implement of electronics

Shown in Fig. 1 is the block diagram of the readout electronics. The electronics is separated into two parts so that it has potential for expansion of more readout channels without changing interface protocol. The Front-End Board (FEB) carries silicon PIN diodes array and an ASIC of SKIROC2 on it. It receives and digitizes the signal from the detectors and supplies high voltage. The FEB is configured by the Data InterFace board (DIF) next to it and drives data to the latter. The data on DIF are then transferred to PC via USB interface after packing process.



Fig. Block diagram of the readout electronics. Mainly consists of FEB and DIF

## ASIC

The core of the FEB is the SKIROC2 ASIC designed for the International Large Detector (ILD) Si-W ECAL2. Fig. 2 presents the schematic illustration of SKIROC2, where 64 channels are integrated on one chip. Each channel is composed of a Charge-Sensitive Amplifier (CSA), two slow shapers with different gains, one fast shaper with a discriminator, a time-to-digital convertor (TDC) for time measurement, three Switched Capacitor Arrays (SCA) of 15 depth to store analog signal and an Analog-to-Digital (ADC) to convert signal from analog to digital.

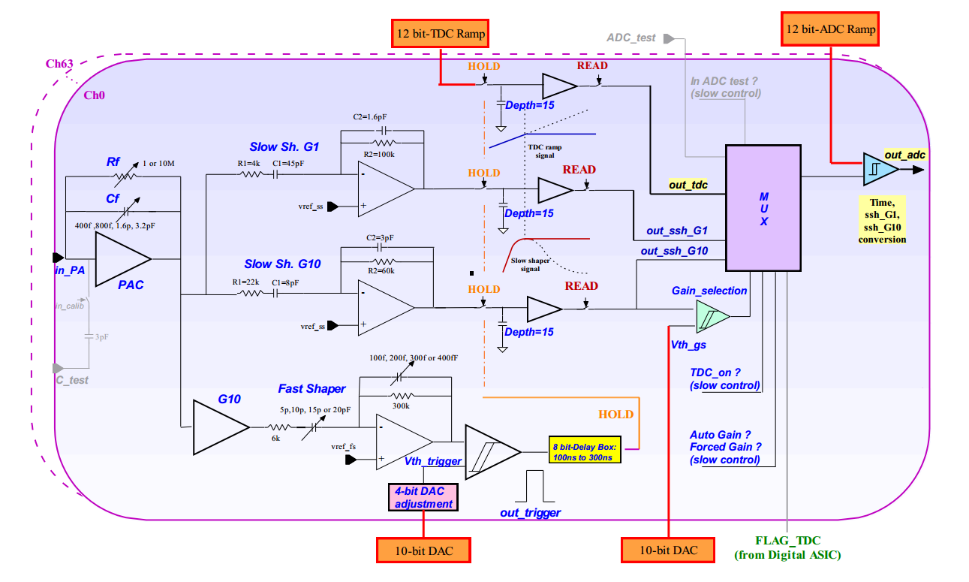


Fig. The schematic illustration of the analog part of SKIROC2 (each channel)

The input signal passes through the CSA with the variable gain set by switchable Feedback Capacitance (Cf) array. The output of CSA is fed to the fast and slow shapers. By comparing fast shaper’s output with a threshold set by an 10 bit on-chip Digital-to-Analog Convertor (DAC), the discriminator generates a trigger signal to hold the voltages at two slow shaper outputs, which are optimized for low-noise charge measurement, on the SCAs. The signals on the SCAs are read out and converted by a 12-bit Wilkinson ADC and a multiplexer, with a bunch ID tagged on a 10 MHz clock, then saved in the on-chip memory.

Benefited from the two different-gain slow shapers and the adjustable gain CSA, the SKIROC2 has a wide dynamic range, ensuring a linear response for equivalent input charge up to +3000 fC, with a noise of 0.2 fC. The peak time is tuneable between 50 ns and 100 ns and the power consumption is about 6 mW per channel. In addition, the SKIROC2 is either self-triggered or ex-triggered. These features meet the requirements of silicon PIN diode. As a result, the SKIROC2 is chosen as readout chip of the electronics.

## Front-end Board

The FEB accommodates one SKIROC2 chip and 64 detectors. The FEB is divided into two parts: Detector-Part and ASIC-Part, so that it is convenient to test different kinds of silicon PIN diodes without redesigning the ASIC-Part. The ASIC-part is designed around the SKIROC2 ASIC. Two ERNI-154744 connectors are responsible for communication with the DIF [6]. All the control signals as well as output data are through these two connectors. There are two kinds of control data buses, depending on the speed; fast control bus and slow control bus. The fast control buses, which work through Low Voltage Differential Signal pairs (LVDS), are directly connected to the control center of SKIRC2. These buses are in charge of SKIROC2’s clock, trigger and reset or validate the SCA. On the other hand, the slow control bus is in a daisy chain cascade and configures the 616-bit registers on the chip to store many configurations such as the feedback capacitance of the CSA and the trigger mode. The output data from SKIROC2 is through Open Collector (OC) gate. Considering the OC gate and daisy chain cascade, it is very convenient to expand the FEB for more ASICs without changing the definition of the connector to DIF.



Fig. Block diagram of Front-end Board. Consists of Detector part and ASIC part.

The Detector-Part carries a silicon PIN diodes array. For now, a kind of silicon PIN diode named S5980 from HAMAMATSU was taken to test the performance of the readout electronics [7]. The active area of the diode is 5 × 5 mm2 and the thickness of depletion layer is 80µm, leading to a result of low reverse voltage demand (about 10 V). The other advantages of the diode are that the dark current is only 100 pA and the thermal capacitance of detector as small as 10 pF. Since the output noise of diode is sensitive to the High Voltage (HV) ripple, the cathode to the diode is connected to a High Voltage (HV) of 13 V, supported by a well-designed Low-DropOut regulator (LDO, TPS7A4700 from Texax Instruments company) with the low power supply ripple rejection of 82 dB. The anode of the diode is directly connected to SKIROC2’s input. The SKIROC2’s input supplies a reference voltage about 1 V to ensure the correct working status of the silicon PIN diode.

## Data Interface

The DIF consists of four main parts; FPGA, connector, power supply and interface.



Fig. Block diagram of logic implemented in the FPGA

The FPGA part is composed of an FPGA (ARTIX7, Xilinx) and a flash programmable read only memory (PROM, N25Q128). The function of the FPGA is to implement the required logic to control the FEB and to communicate with the PC. The logic diagram is presented in Fig. 4. The acquisition module controls the ASIC to work in normal mode and get data saved in SKIROC2. The data transferred into the FPGA is stored in the first-in-first-out (FIFO) memory and transferred to the PC. The trigger module is in charge of generating a trigger when an external trigger is in need, while normally the chip is self-triggered. The calibration module and S-curve module are used to control the ASIC during calibration or testing, which is elaborated below.

The connect part to FEB is via two ERNI-154744 connectors, as mentioned before. The supply part is implemented with a DC input (5V) from outside and several LDO regulators. From this DC supply rail, the analog power supply are generated for DIF and FEB. The interface part is in charge of communicating with PC through a mini-USB port, realized by a USB chip CY7C68013. In addition, an optical transceiver interface is remained for compatibility with other readout device.

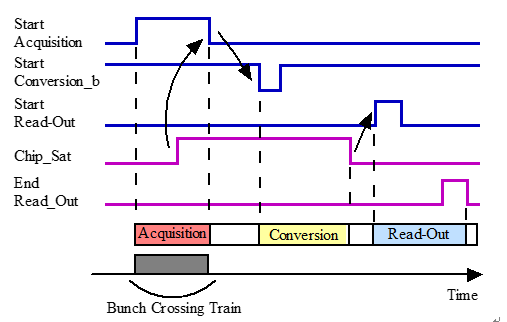


Fig. Global timing control of data acquisition for SKIROC2

The timing control sequence of the main signals during the acquisition is shown in Fig. 5. This global sequencing is made around three signals from FPGA on the DIF: StartAcquisition, StartConversionb and StartReadout. In response to the three signals, the SKIROC2 answers with two signals: Chip\_Sat and End\_Readout. The acquisition is composed of 3 phases: Acquisition, Convertion and Readout. The acquisition phase starts when the StartAcquisition has a rising edge. The SKIROC2 outputs a rising edge of Chip\_Sat signal, informing that the 15-depth SCA array is full. By giving a falling edge of StartConvsionb, the SKIROC2 begins to convert signals from analog to digital. When the conversion is finished, the Chip\_Sat signal falls and a rising of StartReadout signal is sent from DIF to SKIROC2, starting the readout phase. The End\_Readout rises when the transmission is over. It is worth noting that the End\_Readout signal is in daisy chain that the following SKIROC2’s readout phase could be started by this signal, if there are more than one ASIC.

The picture of FEB and DIF is shown in Fig. 6.

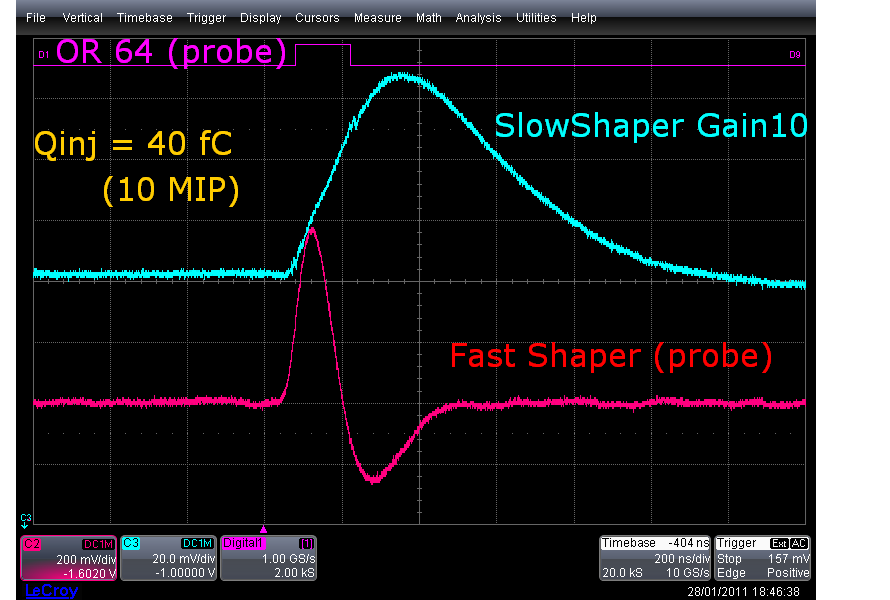


Fig. The digital photograph of FEB and DIF

# Characterization

We have carried out a number of characterizations to assess the performance of the readout electronics. The results of basic output, baseline noise and calibration of SKIROC2, trigger efficiency, X-ray test and cosmic test are presented and discussed below.

## Basic output of SKIROC2



* 1. Baseline and noise
  2. Calibration

## Trigger efficiency

* 1. X-ray test and Cosmic ray test

# Conclusions

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